

Japanese Patent No. 2590931
(Date of Patent: December 19, 1996)

A. Relevance of the Above-identified Document

This document has relevance to Claims 1, 16, 22,
38, 42 and 57 of the present application.

B. Translation of the Relevant Passages of the Document

[CLAIM 1] A signal correction circuit, comprising: an A/D converter for respectively digitizing a video signal and an average brightness level signal obtained by integrating the video signal; a first memory having data to perform log conversion of the digitized video signal; a digital multiplier for multiplying the signal subject to log conversion by the digitized average brightness level signal; a second memory having data to perform exponential conversion of the signal outputted from the digital multiplier; and a multiplier for multiplying the signal subject to exponential conversion by a function of the average brightness level signal, the signal correction circuit further comprising a flip-flop for adjusting timings of the signals provided between circuits.

The present invention has been attained in view of the foregoing problems, and an object of which is to

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provide a signal correction circuit capable of switching correction data in accordance with the size of an APL signal.

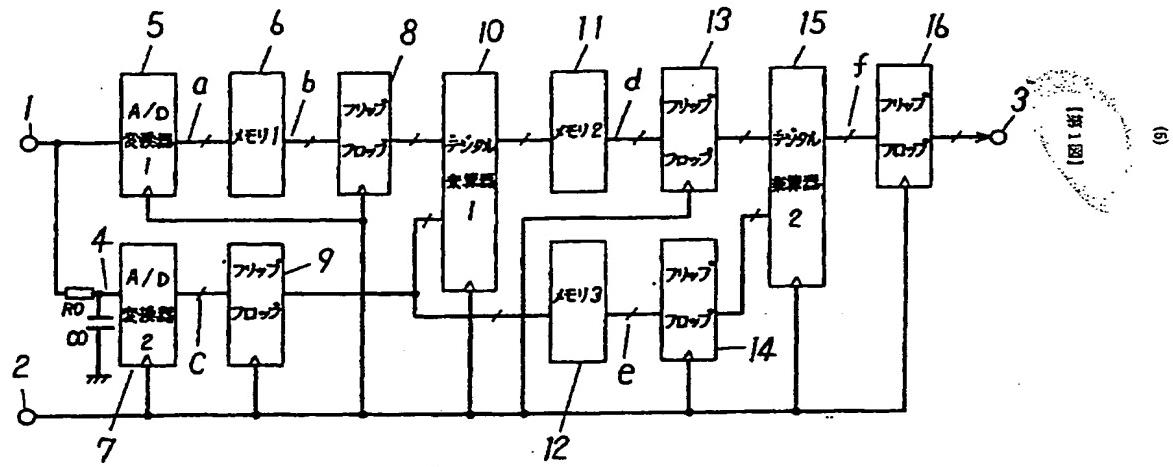
[EFFECTS]

...

In other words, when the block diagram of Fig. 8 is actually developed into a circuit, it is possible to change a way of correction according to a value of γ , that is, APL, as shown in Fig. 7. In the present invention, a memory storing log conversion data, and a memory storing exponential conversion data are respectively adopted as a log converter and an exponential converter.

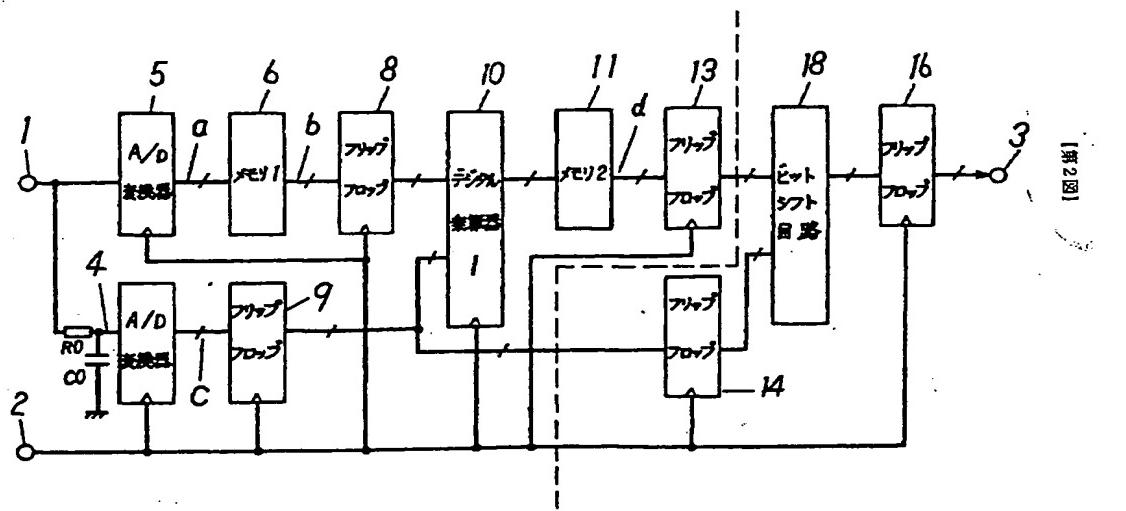
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 2 - クロック入力端子
 3 - 検正されたデジタル
信号出力端子
 4 - APL 信号

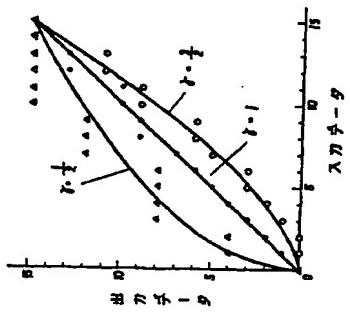


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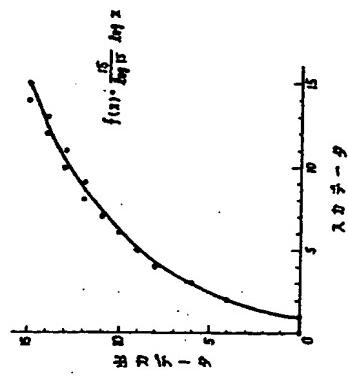
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 4 - APL 信号



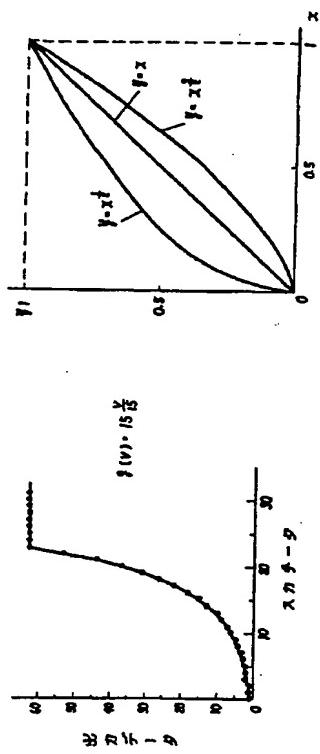
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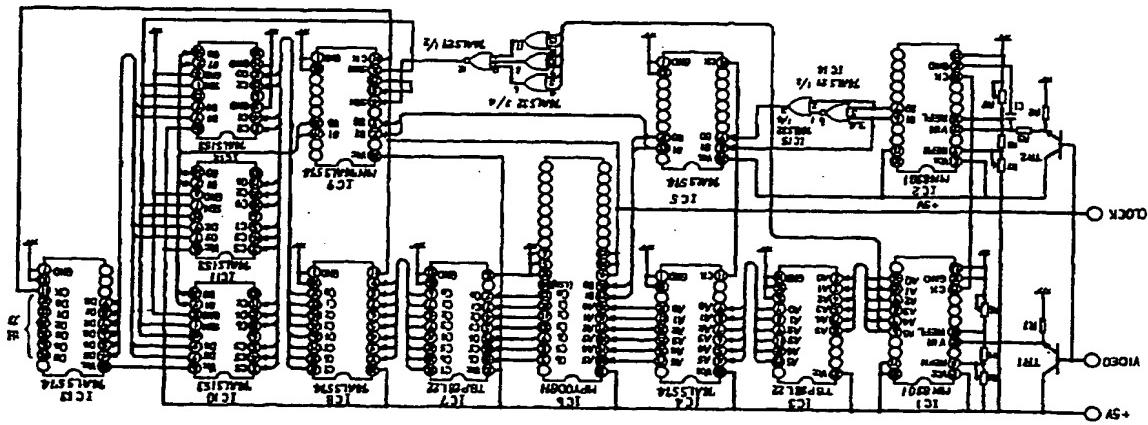
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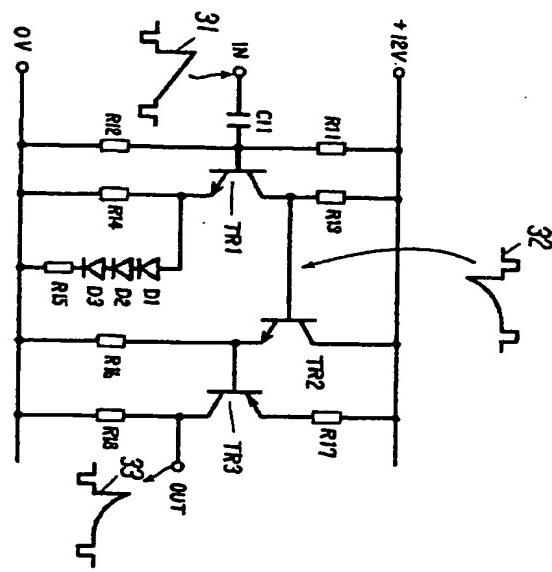


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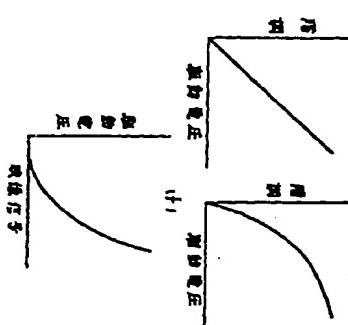
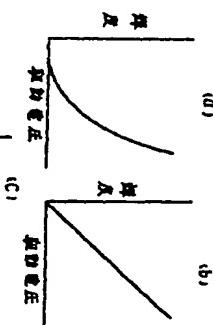
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[第9図]



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[第10図]



フロントページの読み

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